

1        151. A method of operation of a synchronous memory device,  
2 wherein the memory device includes an array of memory cells and a  
3 programmable register, the method of operation of the memory device  
4 comprises:

5        sampling a first operation code synchronously with respect to  
6 a transition of an external clock signal;

7        receiving a binary value synchronously with respect to the  
8 external clock signal, wherein the binary value is representative  
9 of a delay time to transpire before the memory device is to output  
10 data in response to a second operation code, wherein the second  
11 operation code initiates a read operation in the memory device; and

12        storing the binary value in the programmable register in  
13 response to the first operation code.

1        152. The method of claim 151 wherein the first operation code  
2 is included in a control register access request packet.

1        153. The method of claim 152 wherein the first operation code  
2 and the binary value are included in the same control register  
3 access request packet.

1        154. (Amended) The method of claim 151 wherein the delay time  
2 is representative of a number of clock cycles of the external clock  
3 signal.

1 155. The method of claim 154 further including:  
2 receiving the second operation code; and  
3 outputting the data, in response to the second operation code,  
4 after the number of clock cycles of the external clock signal  
5 transpire.

1 156. The method of claim 155 further including sampling  
2 address information synchronously with respect to the external  
3 clock signal.

1 157. The method of claim 156 wherein the address information  
2 and the second operation code are included in a read request  
3 packet.

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1 158. (Amended) The method of claim 151 further including:  
2 receiving block size information, wherein the block size  
3 information is representative of an amount of data to be output;  
4 receiving the second operation code; and  
5 outputting the amount of data in response to the second  
6 operation code, after the delay time transpires.

1 159. The method of claim 158 wherein the block size  
2 information further defines an amount of data to be input in  
3 response to a third operation code, wherein the third operation  
4 code initiates a write operation in the memory device, the method  
5 further including:

6 receiving the third operation code; and

7 inputting the amount of data in response to the third  
8 operation code.

1 160. (Amended) The method of claim 159 wherein the third  
2 operation code is included in a write request packet.

1 161. (Amended) The method of claim 160 wherein the block size  
2 information and the third operation code are included in the same  
3 write request packet.

1 162. The method of claim 155 wherein data is output  
2 synchronously with respect to consecutive rising and falling edge  
3 transitions of the external clock signal.

1 163. The method of claim 151 wherein the first operation code  
2 is received in an initialization sequence after power is applied to  
3 the memory device.

1        164. A method of controlling a synchronous memory device by a  
2 controller, wherein the memory device includes an array of memory  
3 cells and a programmable register, the method of controlling the  
4 memory device comprises:

5        issuing a first operation code to the memory device, wherein  
6 the first operation code initiates an access of the programmable  
7 register in the memory device in order to store a binary value; and

8        providing the binary value to the memory device, wherein the  
9 memory device stores the binary value in the programmable register  
10 in response to the first operation code.

1        165. The method of claim 164 wherein the binary value is  
2 representative of a number of clock cycles of an external clock  
3 signal to transpire before the memory device outputs data in  
4 response to a second operation code.

1        166. The method of claim 165 further including:

2        issuing the second operation code to the memory device; and

3        receiving data output by the memory device after the number of  
4 clock cycles of the external clock signal transpire.

1        167. (Amended) The method of claim 166 further including  
2 providing address information to the memory device synchronously  
3 with respect to the external clock signal.

1        168. The method of claim 167 wherein the address information  
2 and the second operation code are included in a request packet.

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1 169. (Amended) The method of claim 164 further including:  
2 providing block size information to the memory device, wherein  
3 the block size information defines an amount of data to be output  
4 by the memory device in response to a second operation code;  
5 issuing the second operation code to the memory device; and  
6 receiving the amount of data output by the memory device.

1 170. The method of claim 169 wherein the block size  
2 information further defines an amount of data to be input by the  
3 memory device in response to a third operation code, the method  
4 further including:  
5 issuing the third operation code to the memory device; and  
6 providing the amount of data to the memory device.

1 171. The method of claim 164 wherein the first operation code  
2 and the binary value are included in a request packet.

1 172. The method of claim 164 wherein the first operation code  
2 and the binary value are included in the same request packet.

1 173. (Twice Amended) A synchronous memory device including an  
2 array of memory cells, the synchronous memory device comprising:  
3 a clock receiver to receive an external clock signal;  
4 a plurality of input receivers to sample a first operation  
5 code synchronously with respect to a transition of the external  
6 clock signal; and  
7 a programmable register to store a binary value, wherein the  
8 memory device stores the binary value in the programmable register  
9 in response to the first operation code.

1 174. The memory device of claim 173 wherein the binary value  
2 is representative of a number of clock cycles of the external clock  
3 signal, to transpire before the memory device outputs data and  
4 wherein the memory device outputs data in response to a second  
5 operation code.

1 175. (Twice Amended) The memory device of claim 174 further  
2 including a plurality of output drivers to output the data, after  
3 the number of clock cycles of the external clock signal transpire,  
4 in response to the second operation code.

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1 176. (Twice Amended) The memory device of claim 173 further  
2 including a plurality of output drivers to output data, wherein the  
3 data is output in response to a second operation code that  
4 initiates a read operation, and wherein the plurality of output  
5 drivers output a first portion of the data synchronously with  
6 respect to a rising edge transition of the external clock signal

and output a second portion of the data synchronously with respect to a falling edge transition of the external clock signal.

1 177. The memory device of claim 173 wherein the first  
2 operation code is included in a request packet.

1 178. The memory device of claim 173 wherein the first  
2 operation code and the binary value are included in a request  
3 packet.

1 179. (Amended) The memory device of claim 178 wherein the  
2 first operation code and the binary value are included in the same  
3 request packet.

1 180. (Amended) The memory device of claim 173 wherein the  
2 plurality of input receivers are operative to receive a second  
3 operation code, wherein the second operation code initiates a write  
4 operation in the memory device, and wherein the memory device  
5 further includes:  
6 input receivers to input data in response to the second  
7 operation code.

1 181. The method of claim 151 wherein the first operation code  
2 is sampled from an external bus.

1 182. (Amended) The method of claim 181 wherein the external  
2 bus includes a plurality of signal lines, and wherein the binary

3 value and the first operation code are multiplexed over the  
4 plurality of signal lines.

1 183. The method of claim 164 wherein the first operation code  
2 is issued to an external bus.

1 184. (Amended) The method of claim 183 wherein the external  
2 bus includes a plurality of signal lines, and wherein the binary  
3 value and the first operation code are multiplexed over the  
4 plurality of signal lines.

1 185. The memory device of claim 173 wherein the array of  
2 memory cells includes dynamic random access memory cells.

1 186. (Amended) The memory device of claim 173 wherein the  
2 plurality of input receivers sample the first operation code from  
3 an external bus.

1 187. (Amended) The memory device of claim 186 wherein the  
2 external bus includes a plurality of signal lines, and wherein the  
3 first operation code and the binary value are multiplexed over the  
4 plurality of signal lines.

1 188. (Amended) The memory device of claim 187 wherein data,  
2 the first operation code and the binary value are multiplexed over  
3 the plurality of signal lines.

Please ADD the following claims:



1 189. (New) The memory device of claim 173 further including a  
2 delay locked loop, coupled to the clock receiver, to generate an  
3 internal clock signal using the external clock signal.

1 190. (New) The memory device of claim 189 further including a  
2 plurality of output drivers, coupled to the delay locked loop, to  
3 output data in response to the internal clock signal, wherein the  
4 data is accessed from the memory array.

1 191. (New) The memory device of claim 190 wherein the  
2 plurality of output drivers output a first portion of the data  
3 synchronously with respect to a rising edge transition of the  
4 external clock signal, and wherein the plurality of output drivers  
5 output a second portion of the data synchronously with respect to  
6 a falling edge transition of the external clock signal.

1 192. (New) The memory device of claim 191 wherein the memory  
2 device includes a plurality of programmable registers, each  
3 register of the plurality of registers to store a binary value.